Claims

[c1] What is claimed is:

1.A system on chip (SOC) characterized by nitride read only memory (NROM) and read only memory (ROM), the system comprising:

a substrate of a first conductive type, a nitride read only memory (NROM) area, a read only memory area and a periphery area defined on a surface of the substrate;

a plurality of ONO (oxide-nitride-oxide) layers disposed along a first direction in the nitride read only memory area and the read only memory area, a conductive doping area with a second conductive type positioned in the substrate between each ONO layer and used as bit lines of the system on chip;

an oxide layer positioned atop each bit line;

a plurality of word lines covering each ONO layer in the nitride read only memory and the read only memory, the word lines disposed along a second direction and forming a nitride read only memory cell at the intersection of each ONO layer in the nitride read only memory area, and a read only memory cell at the intersection of each ONO layer in the read only memory area;

a plurality of doping areas, each doping area optionally positioned in the substrate at a bottom of a read only memory cell to cause the read only memory cell with the doping area and a read only memory without the doping area to have at least two different threshold voltages, respectively, to present two different storage states;

a plurality of periphery circuit devices positioned on the substrate in the periphery area;

at least one inter-layer dielectric (ILD) and at least one patterned metal interconnect layer subsequently covering the nitride read only memory area, the read only memory area and the periphery area; and

a plurality of plugs positioned in the inter-layer dielectric for electrically connecting each device positioned in the nitride read only memory area, the read only memory area and the periphery area through the metal interconnect layer.

[c2] 2.The system of claim 1 wherein the substrate is a silicon substrate.

[c3] 3.The system of claim 1 wherein two pocket ion implantation areas of the first conductive type are disposed in the substrate at two sides of each bit line.

[c4] 4.The system of claim 1 wherein the first conductive type is a P-type conductive type.

[c5] 5.The system of claim 1 wherein a thickness of the ONO layer ranges from 100 to 250 angstroms (Å).

[c6] 6.The system of claim 1 wherein the ONO layer is formed from a stacked structure comprising a bottom oxide layer with a thickness ranging from 20 to 150 angstroms, a silicon nitride layer with a thickness ranging from 20 to 150 angstroms, and a top oxide layer with a thickness ranging from 50 to 150 angstroms.

[c7] 7.The system of claim 1 wherein each word line is composed of a polysilicon layer.

[c8] 8.The system of claim 7 wherein a polysilicide layer is formed on a surface of the polysilicon layer.

[c9] 9.The system of claim 1 wherein the read only memory is a mask read only memory (mask ROM, MROM).

[c10] 10.The system of claim 1 wherein the plurality of doping areas are formed by utilizing an ion implantation process capable of optionally implanting ions into the substrate at a bottom of a read only memory cell to form ROM code.

[c11] 11.A system on chip (SOC) characterized by nitride read only memory (NROM) and read only memory(ROM), the system comprising:
a substrate of a first conductive type, a nitride read only memory(NROM) area, a read only memory area and a periphery area defined on a surface of the substrate;
a plurality of ONO (oxide-nitride-oxide) layers positioned on the nitride read only memory area, the ONO layers disposed along a first direction;
a plurality of gate oxide layers positioned on the read only memory area, the gate oxide layers disposed along the first direction;

a plurality of conductive doping areas of a second conductive type positioned in the substrate between each ONO layer and each gate oxide layer, the conductive doping areas being used as bit lines of the system on chip;

an oxide layer positioned atop each bit line;

a plurality of word lines covering each ONO layer in the nitride read only memory area and the gate oxide layers in the read only memory area, the word lines disposed along a second direction and forming a nitride read only memory cell at the intersection of each ONO layer in the nitride read only memory area, and a read only memory cell at the intersection of each gate oxide layer in the read only memory area;

a plurality of doping areas, each doping area optionally positioned in the substrate at a bottom of a read only memory cell to cause the read only memory cell with the doping area and a read only memory without the doping area to have at least two different threshold voltages, respectively, to present two different storage states;

a plurality of periphery circuit devices positioned on the substrate in the periphery area;

at least one inter-layer dielectric (ILD) and at least one patterned metal interconnect layer subsequently covering the nitride read only memory area, the read only memory area, and the periphery area; and

a plurality of plugs positioned in the inter-layer dielectric for electrically connecting each device positioned in the nitride read only memory area, the read only memory area, and the periphery area through the metal interconnects layer.

[c12] 12.The system of claim 11 wherein the substrate is a silicon substrate.

[c13] 13.The system of claim 11 wherein two pocket ion implantation areas of the first conductive type are disposed in the substrate at two sides of each bit line.

[c14] 14.The system of claim 11 wherein the first conductive type is a P-type conductive type.

[c15] 15.The system of claim 11 wherein a thickness of the ONO layer ranges from 100 to 250 angstroms (Å).

[c16] 16.The system of claim 11 wherein the ONO layer is formed from a stacked structure comprising a bottom oxide layer with a thickness ranging from 20 to 150 angstroms, a silicon nitride layer with a thickness ranging from 20 to 150 angstroms, and a top oxide layer with a thickness ranging from 50 to 150 angstroms.

[c17] 17.The system of claim 11 wherein each word line is composed of a polysilicon layer.

[c18] 18.The system of claim 17 wherein a polysilicide layer is formed on the surface of the polysilicon layer.

[c19] 19.The system of claim 11 wherein the read only memory is a mask read only memory (mask ROM, MROM).

[c20] 20.The system of claim 11 wherein the plurality of doping areas are formed by utilizing an ion implantation process that is capable of optionally implanting ions into the substrate at a bottom of a read only memory cell to form ROM code.